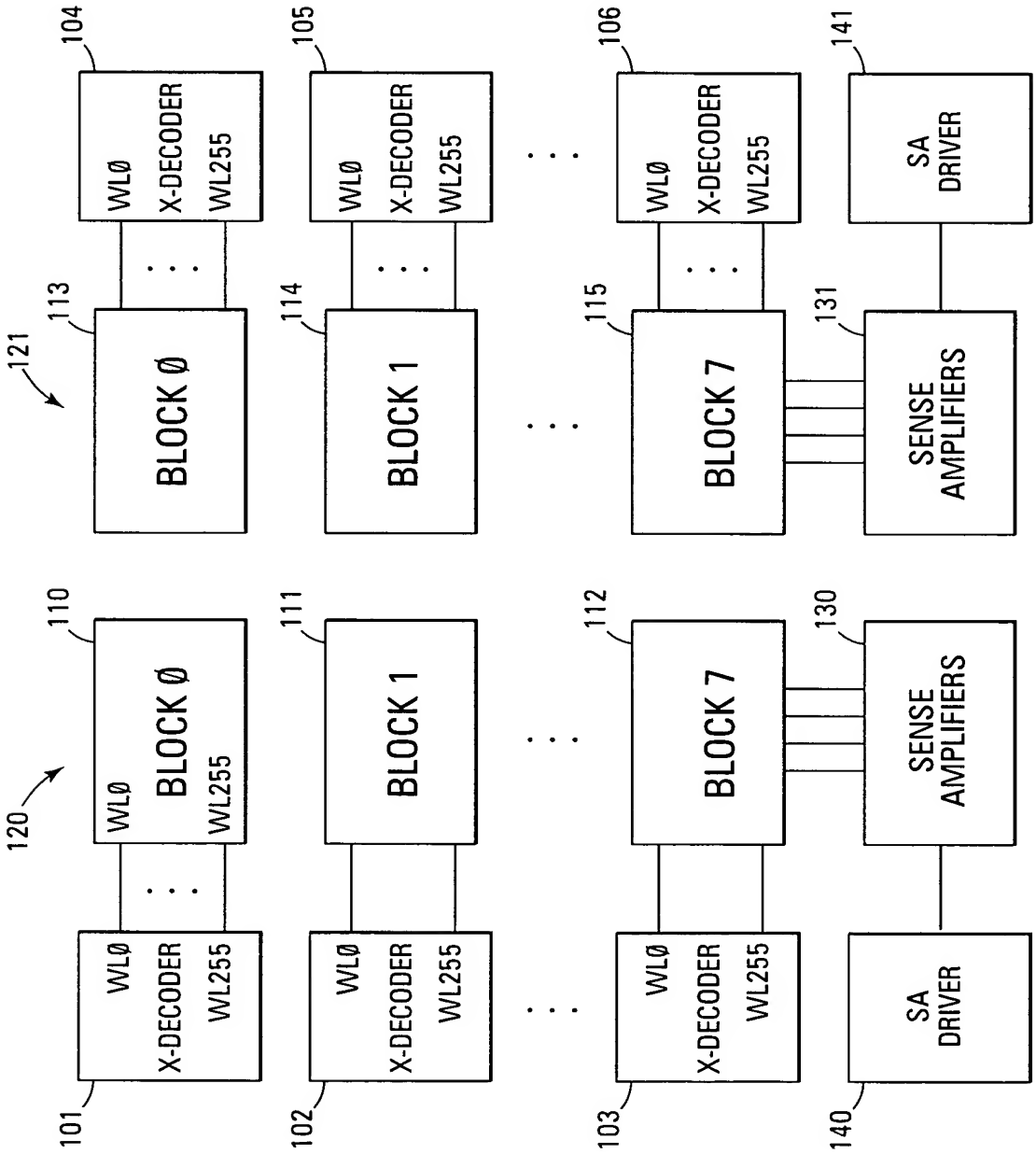

Fig. 1
Prior Art

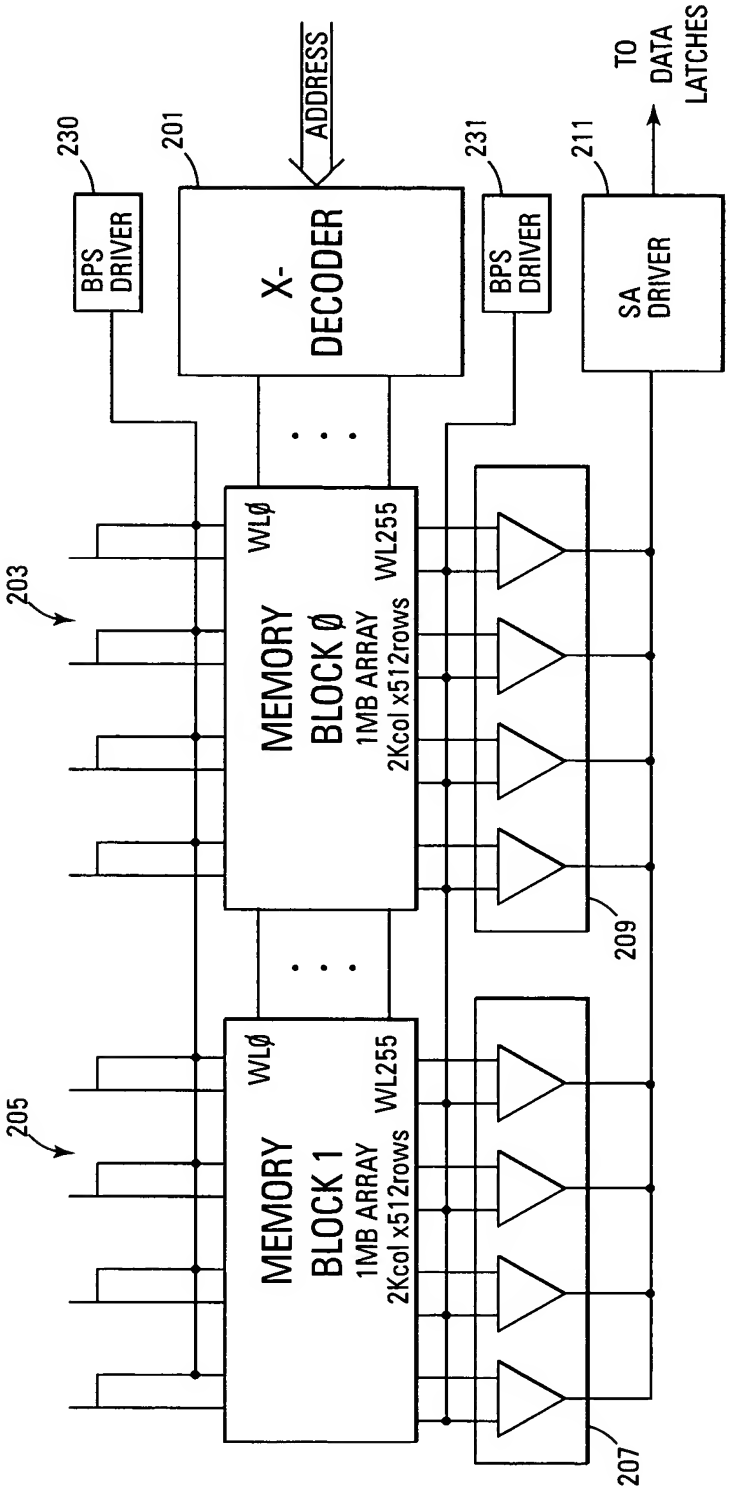
230
BPS DRIVER
201
ADDRESS
X-DECODER
231
BPS DRIVER
211
TO DATA LATCHES
SA DRIVER
203
MEMORY BLOCK Ø
1MB ARRAY
2Kcol x512rows
WLØ
WL255
209
205
MEMORY BLOCK 1
1MB ARRAY
2Kcol x512rows
WLØ
WL255
207

Fig. 2

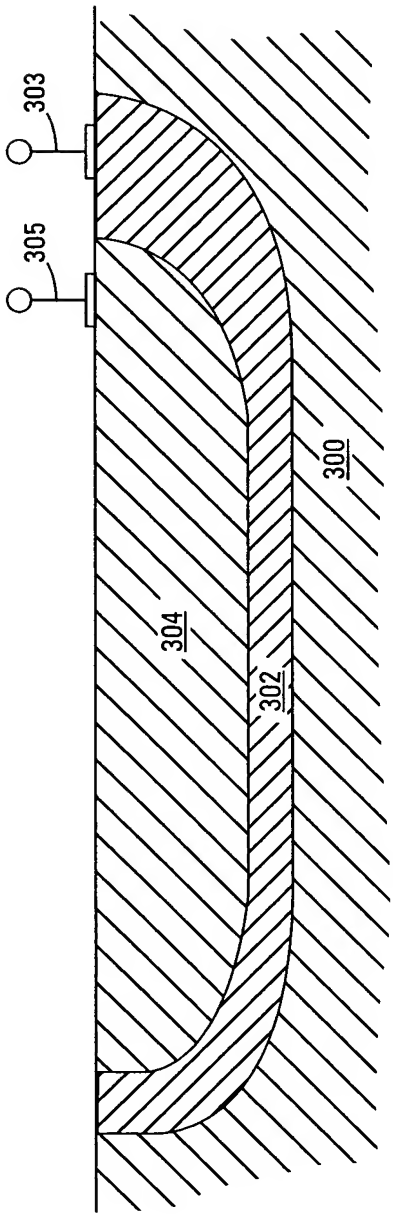

Fig. 3

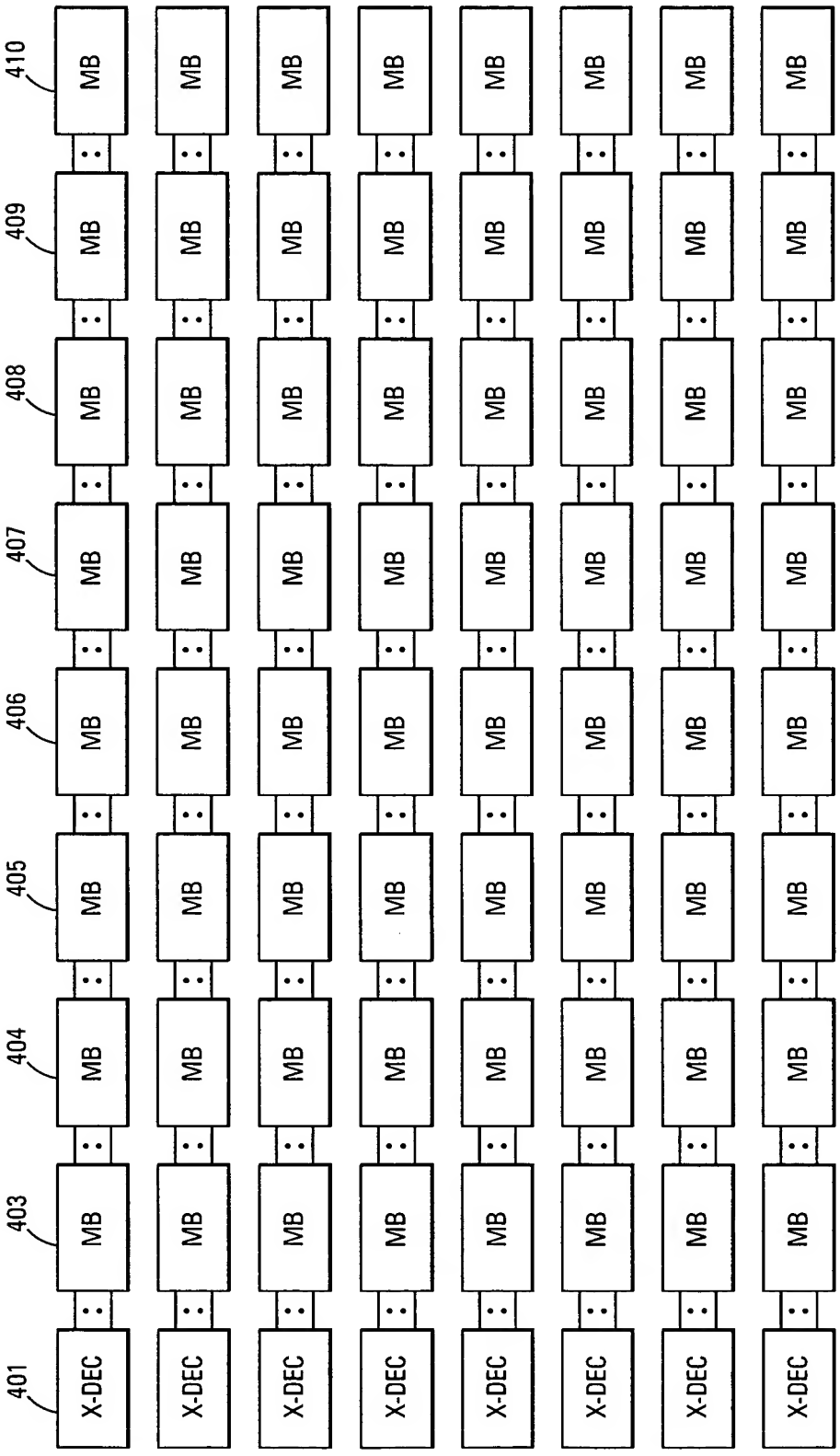

Fig. 4

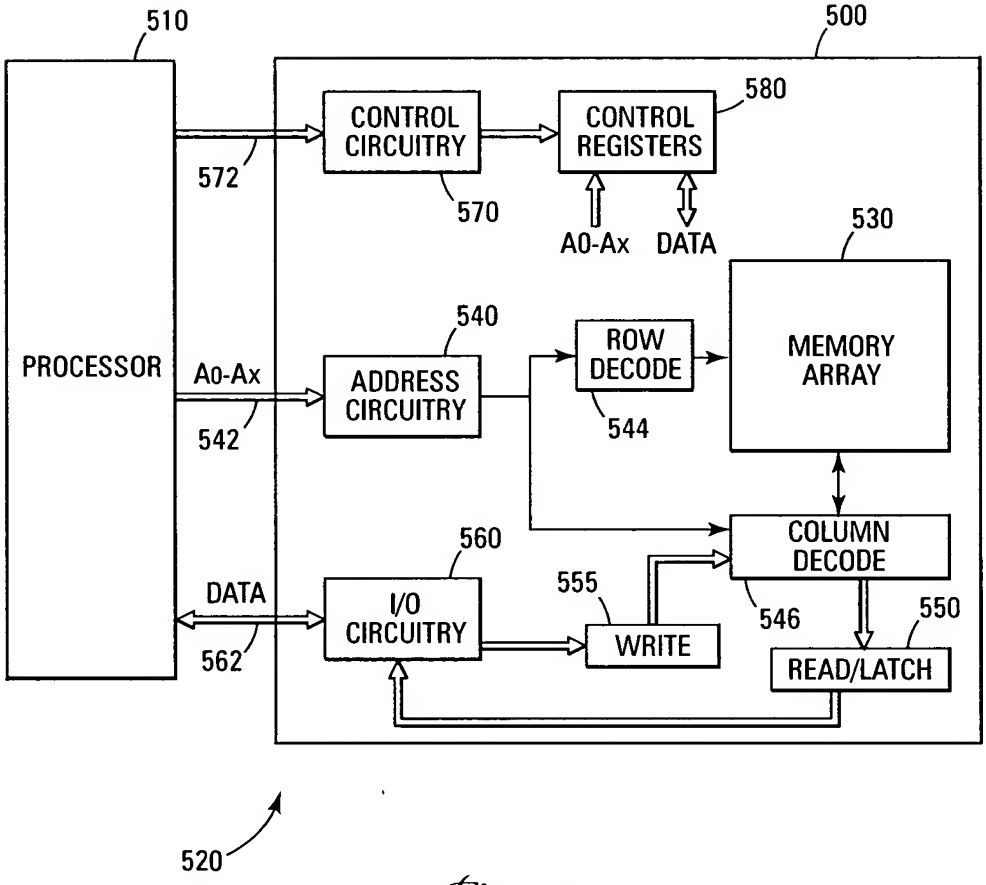
510
500
CONTROL CIRCUITRY
CONTROL REGISTERS
580
572
570
A0-Ax
DATA
530
PROCESSOR
A0-Ax
ADDRESS CIRCUITRY
540
ROW DECODE
MEMORY ARRAY
542
544
COLUMN DECODE
560
DATA
I/O CIRCUITRY
555
WRITE
546
550
562
READ/LATCH
520

Fig. 5